(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 672 898 B1

(12) EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention of the grant of the patent:
26.05.1999 Bulletin 1999/21

(51) Int Cl.6: **G01L 9/06**, G01L 9/00

(21) Application number: 95103970.0

(22) Date of filing: 17.03.1995

(54) **Semiconductor pressure sensor with polysilicon diaphragm and single-crystal gage elements and fabrication method therefor**

Halbleiter-Druckwandler mit Polysilizium-Membran und Einkristall-Dehnungsmesstreifen und Herstellungsverfahren dazu

Capteur semi-conducteur de pression avec membrane en polysilicium et jauges de contraintes monocristaux et son procédé de fabrication

(84) Designated Contracting States:
DE FR GB

(30) Priority: 18.03.1994 US 210422

(43) Date of publication of application:
20.09.1995 Bulletin 1995/38

(73) Proprietor: THE FOXBORO COMPANY
Foxboro, MA 02035-2099 (US)

(72) Inventor: Fung, Clifford D.
Mansfield, Massachusetts 02048 (US)

(74) Representative:
Blumbach, Kramer & Partner GbR
Radeckestrasse 43
81245 München (DE)

(56) References cited:
DE-A- 2 429 894
DE-A- 3 319 605
US-A- 4 721 938

EP 0 672 898 B1

Description

Background

[0001] This invention relates to semiconductor pressure sensors, and to improved methods for manufacturing such devices.

[0002] Semiconductor pressure sensors and strain gages are commonplace today. Their extremely small size, less than 0.125 inch (3.175 mm) in any dimension, is typical. High durability to outside forces makes these devices popular for the pressure measurement needs of hydraulic and aerodynamics forces, among other applications.

[0003] Typically, semiconductor pressure sensors contain a diaphragm of one or more silicon layers for deflecting in response to opposing pressure environments, and piezoresistive elements that are configured for sensing the direction and/or magnitude of diaphragm deflection.

[0004] The manufacture of these sensors makes the diverse range of devices available today and one aspect of the invention provides improvements in that manufacture. Because high temperature stability is often required, improvements relating to sensor heat stability is an active research area. Dielectric isolation is one technique which increases stability. The dielectric ideally isolates semiconductor piezoresistive elements from the diaphragm, the support structure, and other piezoresistive elements. Silicon dioxide, SiO2, exemplifies a known dielectric that maintains a nearly constant resistance over significant temperature changes.

[0005] The type of silicon used in the pressure sensor is also important. Single-crystal silicon and polycrystalline silicon materials have different properties that influence mechanical strength, sensitivity, and even manufacturability.

[0006] Despite the advances made in semiconductor physics, pressure sensors with improved temperature stability and higher pressure sensitivity are sought, particularly for use in hostile environments Devices available today generally have limited sensitivity and dielectric isolation, that restrict stability and high temperature operation.

[0007] In U.S. Patent No. 4,672,354 for "Fabrication of Dielectrically Isolated Fine Line Semiconductor Transducers and Apparatus", for example, glass is used as an insulator and as a bonding agent. Such a pressure transducer is difficult to manufacture, and has other undesirable characteristics.

[0008] In U.S. Patent No. 4,721,938 single-crystal silicon piezoresitive sensing elements are arranged at a surface of a polysilicon diaphragm opposite to the silicon support structure.

[0009] With this background, an object of this invention is to provide improved semiconductor pressure sensors and associated methods, and in particular, for uses which require high temperature stability and high sensitivity.

[0010] Another object of the invention is to provide a high sensitivity semiconductor pressure sensor which is easier to manufacture than competitive existing sensors.

[0011] A further object of this invention is to provide a semiconductor pressure sensor, and a related method of manufacture, for dielectrically isolating single crystal silicon sensors.

[0012] Other objects of the invention are evident in the description which follows.

Summary of the Invention

[0013] The invention features a semiconductor pressure sensor as defined in claim 1. Such a sensor has a polysilicon diaphragm and a supporting etched silicon substrate. A piezoresistive single-crystal gage element of p-type implants is disposed adjacent a first side of the diaphragm and is dielectrically isolated from other elements of the sensor by a layer of silicon oxide formed by oxygen ion implantation. An electrical interconnection connects the gage element to external electronics.

[0014] Preferably, the silicon substrate and the oxygen ion implantation form a common silicon-on-insulator (SOI) wafer, and additional surface-annealed silicon forms the piezoresistive gage element. The gage element is further isolated by the silicon oxide layer within the SOI wafer.

[0015] The piezoresistive gage element is disposed between the diaphragm and the substrate. This facilitates the manufacturing process and allows the substrate to be etched on a backside, away from the rest of the pressure sensor. A farther dielectric isolator, of passivating nitride, can provide additional electrical isolation for the p-type piezoresistive gage element.

[0016] The invention also features a method for manufacturing semiconductor pressure sensors as defined in claim 4. The method includes the steps of forming a single-crystal piezoresistive gage element by boron ion implantation and etching the surface of annealed silicon of a silicon-on-insulator (SOI) wafer. The wafer includes a silicon substrate, a first oxygen ion implantation to form silicon oxide, and the aforementioned surface annealed silicon. Polysilicon is deposited on the gage element to form a diaphragm with opposing first and second surfaces, with the piezoresistive gage element adjacent the first surface. Evaporated metal, e.g., aluminum, is deposited and etched to provide an external electrical connection to the piezoresistive gage element. The silicon substrate, as part of the SOI wafer, is then etched to provide a backside pressure port such that the diaphragm can deflect in response to a pressure difference between the first and second surfaces. A nitride deposition layer is preferably deposited on the piezoresistive gage element to provide additional dielectric isolation.

[0017] These and other features of a sensor accord-

ing to the invention provide several advantages. In particular, the dielectric isolation of the silicon oxide layer provides the sensor with high operating stability and high temperature capability, and also provides an etch stop for backside etching of the pressure port. By using single-crystal silicon as the piezoresistive gage element, the sensor provides relatively high sensitivity at low pressure differentials and is relatively easy to manufacture. This enables the device to be coupled more effectively with digital electronics, with the potential for meeting high-performance, intelligent pressure transmitter needs. The polysilicon diaphragm provides improved robustness and improved control of diaphragm thickness as compared to sensors employing single-crystal diaphragms. Further, the configuration of the sensor provides protection of the gage elements because they are sandwiched between the polysilicon diaphragm and the silicon oxide isolation layer and the silicon substrate.

[0018] These and other aspects and advantages will become apparent in the following description.

Brief Description of the Drawings

[0019] For a fuller understanding of the nature and objects of the invention, reference should be made to the following detailed description and the accompanying drawings, in which:

FIGURE 1 is a cross-sectional view of a semiconductor pressure sensor constructed in accordance with the invention;

FIGURE 1A illustrates a schematic top view of the pressure sensor of FIGURE 1;

FIGURE 2 is a cross-sectional view of an illustrative silicon-on-insulator (SOI) wafer;

FIGURE 2A shows the SOI wafer of FIGURE 2 implanted selectively with boron ions to create p-type regions as sensing resisters and p+ regions for interconnection

FIGURE 2B shows the wafer of FIGURE 2A after etching to form P+ interconnection and P-type sensing resistors;

FIGURE 2C shows the wafer of FIGURE 2B with an additional nitride deposition and etching;

FIGURE 2D shows the wafer of FIGURE 2C with a polysilicon deposition and etching to form a polysilicon diaphragm; and

FIGURE 2E schematically illustrates in a cross-sectional side view the pressure sensor of FIGURE 1 in an etching fixture for etching the silicon substrate.

Description of Illustrated Embodiments

[0020] FIGURES 1 and 1A show a semiconductor pressure sensor 10 with an etched silicon substrate 12 supporting a polysilicon diaphragm 14 at the top, in a configuration that facilitates the manufacturing process. The substrate 12 includes a localized region of oxygen ion implantation to form a silicon oxide layer 16. The sensor 10 is annealed and implanted with boron ions, in selected localized regions, and selectively etched, to form p-type gage piezoresistors 18 and p+ interconnections 20. A nitride deposition layer 22 preferably passivates the p-type piezoresistors 18. Metal contacts 24 provide electrical communication to the p+ interconnections 20 and provide a way to externally connect the sensor 10 to a further electrical device.

[0021] The electrical signals produced at the metal contacts 24 are an indication of the pressure differential across the diaphragm 14, i.e., between pressure environments 28 and 30. The electrical signals produced by the p-type gage elements 18 are indicative of a resistance change functionally dependent upon the local stress distribution of the diaphragm 14. The etched portion 31 of the substrate 12 defines a pyramidal pressure port 32, which exposes the diaphragm 14 to the pressure environment 28, and the substrate 12 supports the sensor 10 at mounting points 26.

[0022] The FIGURE 1 showing of the pressure sensor 10, and the similar drawings in FIGURES 2-2E, contain exaggerated proportions for clarity of illustration. For example, the silicon oxide layer 16, FIGURE 1, is typically 0.45 micron thick, and the etched piezoresistive gage elements 18 are typically 0.4 micron thick.

[0023] FIGURE 1A is a diagrammatic top view (not to scale) of the sensor 10 of FIGURE 1, and, for clarity of illustration, shows the p+ interconnections 20 and the p-type piezoresistive elements 18 above the diaphragm when in fact they are beneath it. The gage elements 18, which preferably inter-connect and form a conventional Wheatstone bridge configuration at the inner ends of the p+ interconnections 20, are located over the edges of the pressure port 32, as defined by the edge of the substrate silicon etched portion 31 (FIGURE 1). The metal contacts 24, for connecting the sensor 10 to external electronics, are located at the outer ends of the p+ interconnections 20. A disturbance to this bridge circuit, caused by pressure-induced diaphragm deflection, provides a measurable voltage signal at the contacts 24.

[0024] In order to produce maximal additive read-out of diaphragm movement, the gage elements 18 are preferably oriented in a push-pull configuration. In this configuration, each of the elements 18 is oriented relative to the edge of the diaphragm 14 that is nearest to the element, with two of the elements 18 arranged perpendicular to the edge, and the other two elements arranged parallel to the edge.

[0025] The sensor 10 can include aluminum bond pads 34 and 35, as also illustrated in FIGURE 1A. Typ-

ically, the pads 34 are connected to a voltage source, and the pads 35 provide a measurement signal indicative of pressure on the diaphragm 14.

[0026] FIGURES 1 and 1A show one preferred embodiment of the invention in its overall operative state. FIGURES 2-2E illustrate manufacturing stages to fabricate the sensor 10 of FIGURE 1.

[0027] FIGURE 2 illustrates a general silicon-on-insulator (SOI) wafer 40. A silicon substrate 12 is implanted with oxygen ions 44 to create a buried silicon oxide layer 16 which typically is approximately 0.45 micron thick. Ion implantation is a known process and usually includes an ion source, focusing elements, an acceleration tube and a mass analyzer. The silicon oxide layer 16 can be formed precisely with known technologies and forms a dielectric isolator which inhibits leakage from subsequently-formed piezoresistive gage elements amongst themselves or to other electrically conductive elements of the wafer 40. A single-crystal silicon surface layer 42 is formed on the silicon oxide layer 16 by an annealing process, also well known, to a thickness typically of approximately 0.2 to 0.4 micron. Surface silicon annealing typically occurs over one to two hours in a dry nitrogen environment at a temperature over 1000°C.

[0028] The SOI wafer 40 of FIGURE 2, formed by oxygen ion implantation and annealing, is commercially available. The SOI structure provides improved dielectric isolation when combined with further features of the invention. Further, the practice of the invention is not limited to the implanted silicon oxide layer 16 of FIGURES 1, 1A and 2; other silicon oxide forms are acceptable as dielectric isolators.

[0029] The SOI wafer 40 of FIGURE 2 is selectively doped with boron ions 46, as illustrated in FIGURE 2A, at the single-crystal silicon surface layer 42, to prepare for the formation of p-type piezoresistive gage elements and p+ interconnection. The piezoresistive gage elements 18 and interconnections 20 are formed by etching the doped single-crystal silicon, as illustrated in FIGURE 2B. Preferably, but not required, nitride deposition forms a passivation layer 22, as shown in FIGURE 2C; and selective etching of the layer 22 provides access to the contact 24 of FIGURE 2D. The passivation layer 22 is functionally used to protect the gage elements from environmental factors such as humidity or contamination.

[0030] The sensing diaphragm 14 of FIGURE 2D is formed on the passivation layer 22 by polysilicon deposition. Selective etching of the diaphragm 14 shapes the diaphragm boundary and provides access to the metal contact 24, which is thereafter formed by etching on each p+ interconnection 20, as exemplified in FIGURE 2C, and by evaporated aluminum deposition. Other high temperature metals can also be used for the interconnections.

[0031] FIGURE 2E illustrates a final step in the illustrated embodiment for producing the sensor 10 of FIGURE 1 (for illustrative purposes, only one metal contact 24 is shown in FIGURES 2D and 2E). In particular, the silicon substrate 12 is etched with an appropriate etchant at the illustratively pyramidal etch region 49, while the front of the sensor, e.g., the diaphragm 14, is protected from the etchant by a conventional fixture 50, illustrated as having an O-ring interface seal 52.

[0032] Those skilled in the art will appreciate that modifications to the above description, and to the illustrated structures and procedures can be made without departing from the scope of the invention as it is defined in the claims. For example, sensor 10 of FIGURE 1 is readily configured to external lead-out pads, and connected to a Whetstone bridge configuration as is well-known to those skilled in the art. Further, and without limitation, layer thicknesses and multiple oxygen ion implantations, as illustrated in FIGURES 1-2, can be changed and implemented through a variety of means.

[0033] It is thus seen that the invention efficiently attains the objects set forth above, among those apparent in the preceding description. In particular, the invention provides a high sensitivity semiconductor pressure sensor with relatively high temperature stability.

[0034] It is accordingly intended that all matter contained in the above description or shown in the accompanying drawings be interpreted as illustrative, rather than as limiting.

Claims

1. Semiconductor pressure sensor apparatus comprising

   A. a polysilicon diaphragm (14) having opposed first and second surfaces,
   B. an etched silicon substrate (12) supporting said diaphragm at said first surface for deflection of said diaphragm in response to a pressure difference between said first and second surfaces,
   C. first means (18) forming single-crystal silicon piezoresistive sensing means mounted with said first surface of said polysilicon diaphragm for sensing deflection of said diaphragm,
   D. dielectric isolation means (16, 22) for dielectrically isolating said sensing means (18), said isolation means including silicon oxide implantation, and
   E. first interconnection means (20) in circuit with said sensing means (18) for external electrical connection to said pressure sensor.

2. Semiconductor pressure sensor apparatus according to claim 1 wherein said sensing means (18) is disposed substantially between said diaphragm (14) and said substrate (12).

3. Semiconductor pressure sensor apparatus accord-

ing to claim 1 wherein

A. said first means (18) includes silicon with a p-type implant, and

B. said dielectric isolation means (16, 22) further comprises a nitride deposition for passivation of said p-type implant of said first means (18).

4. A method for manufacturing a semiconductor pressure sensor, said method comprising the successive steps of

A. providing a silicon-on-insulator wafer, said wafer including a silicon substrate, a first silicon oxide implantation, and surface annealed silicon,

B. forming a dielectrically isolated single-crystal silicon piezoresistive gage element in said surface silicon by successive boron ion implantation and etching,

C. depositing polysilicon on said gage element to form a diaphragm having opposed first and second surfaces, said first surface being adjacent said piezoresistive gage element,

D. forming an external connector by metal evaporation and etching, said external connector being in circuit with said gage element for providing an external electrical connection to said sensor, and

E. etching said substrate to configure said diaphragm for deflection in response to a pressure difference between said first and second surfaces.

5. A method according to claim 4 comprising the further step of depositing passivation nitride on said piezoresistive gage element before said polysilicon-depositing step for providing additional dielectric isolation of said gage element.

Patentansprüche

1. Halbleiterdrucksensoreinrichtung mit

A. einer aus Polysilizium bestehenden Membran (14), die sich gegenüberliegende erste und zweite Oberflächen aufweist,
B. einem geätzten Substrat (12) aus Silizium, das die Membran an der ersten Oberfläche so abstützt, daß die Membran in Abhängigkeit von einer Druckdifferenz zwischen der ersten und der zweiten Oberfläche auslenkbar ist,
C. einer ersten Einrichtung (18), die eine piezoresistive Erfassungseinrichtung aus einkristallinem Silizium bildet und an der ersten Oberfläche der aus Polysilizium bestehenden Membran zum Erfassen einer Auslenkung der Membran angeordnet ist,
D. einer dielektrischen Isolationseinrichtung (16, 22) zum dielektrischen Isolieren der Erfassungseinrichtung (18), wobei die Isolationseinrichtung eine Siliziumoxidimplantierung enthält, und
E. einer ersten Verbindungseinrichtung (20), die mit der Erfassungseinrichtung (18) verschaltet ist und für die externe elektrische Verbindung mit dem Drucksensor dient.

2. Halbleiterdrucksensoreinrichtung nach Anspruch 1, bei der die Erfassungseinrichtung (18) im wesentlichen zwischen der Membran (14) und dem Substrat (12) angeordnet ist.

3. Halbleiterdrucksensoreinrichtung nach Anspruch 1, bei dem

A. die erste Einrichtung (18) Silizium mit einer Implantierung des Leitungstyps p umfaßt, und
B. die dielektrische Isolationseinrichtung (16, 22) weiterhin eine Nitridbeschichtung zum Passivieren der Implantierung des Leitungstyps p der ersten Einrichtung (18) aufweist.

4. Verfahren zum Herstellen eines Halbleiterdrucksensors, wobei das Verfahren die aufeinanderfolgenden Schritte aufweist:

A. Bereitstellen eines Silizium-auf-Isolator-Wafers, wobei der Wafer ein Substrat aus Silizium, eine erste Siliziumoxidimplantierung und ein oberflächengeglühtes Silizium umfaßt,
B. Ausbilden eines dielektrisch isolierten, piezoresistiven, aus einkristallinem Silizium bestehenden Fühlerelements in dem Oberflächensilizium durch sukzessives Implantieren und Ätzen,
C. Aufbringen von Polysilizium auf dem Fühlerelement zur Bildung einer Membran, die sich gegenüberliegende erste und zweite Oberflächen aufweist, wobei die erste Oberfläche in der Nähe des piezoresistiven Fühlerelements angeordnet ist,
D. Ausbilden eines externen Verbinders durch Aufdampfen von Metall und Ätzen, wobei der externe Verbinder mit dem Fühlerelement verschaltet ist, um hierdurch eine externe elektrische Verbindung mit dem Sensor bereitzustellen, und
E. Ätzen des Substrats zur Formgebung der

Membran für eine Auslenkung in Abhängigkeit von einer Druckdifferenz zwischen der ersten und der zweiten Oberfläche.

5. Verfahren nach Anspruch 4, das den weiteren Schritt des Aufbringens von passivierendem Nitrid auf dem piezoresistiven Fühlerelement vor dem Schritt des Aufbringens von Polysilizium umfaßt, um hierdurch eine zusätzliche dielektrische Isolierung des Fühlerelements zu schaffen.

Revendications

1. Appareil détecteur de pression à semi-conducteur comprenant :

   A. un diaphragme de polysilicium (14) ayant une première et une deuxième surfaces opposées,
   B. un substrat de silicium gravé (12) soutenant ledit diaphragme au niveau de ladite première surface pour une déflexion dudit diaphragme en réponse à une différence de pression entre lesdites première et deuxième surfaces,
   C. un premier moyen (18) formant un moyen de détection piézorésistif à silicium monocristallin monté avec ladite première surface dudit diaphragme de polysilicium afin de détecter la déflexion dudit diaphragme,
   D. un moyen d'isolation diélectrique (16, 22) pour isoler diélectriquement ledit moyen de détection (18), ledit moyen d'isolation comprenant l'implantation d'oxyde de silicium, et
   E. un premier moyen d'interconnexion (20) en circuit avec ledit moyen de détection (18) en vue d'une connexion électrique externe audit détecteur de pression.

2. Appareil détecteur de pression à semi-conducteur selon la revendication 1, dans lequel ledit moyen de détection (18) est disposé essentiellement entre ledit diaphragme (14) et ledit substrat (12).

3. Appareil détecteur de pression à semi-conducteur selon la revendication 1, dans lequel

   A. ledit premier moyen (18) comprend du silicium avec un implant de type p, et
   B. ledit moyen d'isolation diélectrique (16, 22) comprend de plus un dépôt de nitrure en vue de la passivation dudit implant de type p dudit premier moyen (18).

4. Procédé pour fabriquer un détecteur de pression à semi-conducteur, ledit procédé comprenant les étapes successives consistant :

   A. à fournir une plaquette de silicium-sur-isolant, ladite plaquette comprenant un substrat de silicium, une première implantation d'oxyde de silicium et du silicium superficiel recuit,
   B. à former un élément de jauge piézorésistive de silicium monocristallin diélectriquement isolé dans ledit silicium superficiel au moyen d'une implantation d'ions de bore et de gravure successives,
   C. à déposer du polysilicium sur ledit élément de jauge afin de former un diaphragme ayant une première et une deuxième surfaces opposées, ladite première surface étant adjacente audit élément de jauge piézorésistif.
   D. à former un connecteur externe au moyen d'une vaporisation de métal et d'une gravure, ledit connecteur externe étant en circuit avec ledit élément de jauge afin d'offrir une connexion électrique externe audit détecteur, et
   E. à graver ledit substrat afin de configurer ledit diaphragme pour une déflexion en réponse à une différence de pression entre lesdites première et deuxième surfaces.

5. Procédé selon la revendication 4, comprenant l'étape supplémentaire consistant à déposer un nitrure de passivation sur ledit élément de jauge piézorésistif avant ladite étape de dépôt de polysilicium afin d'offrir une isolation diélectrique supplémentaire dudit élément de jauge.

FIGURE 1

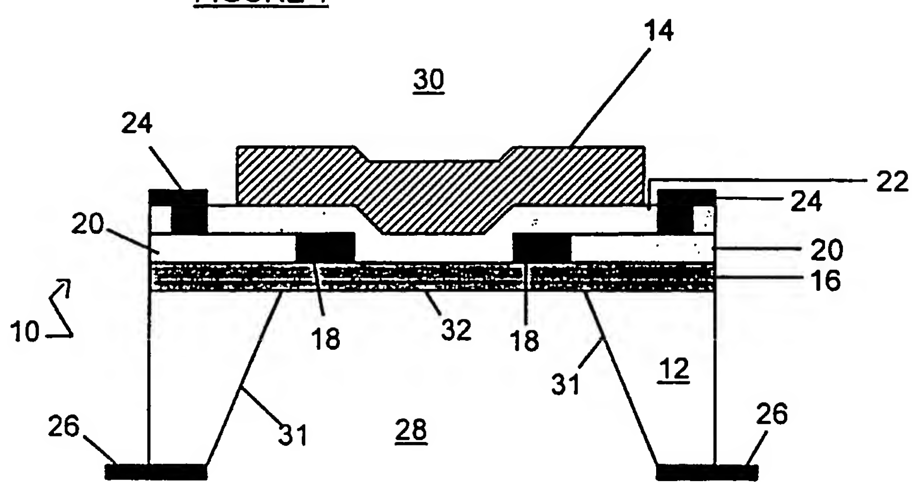
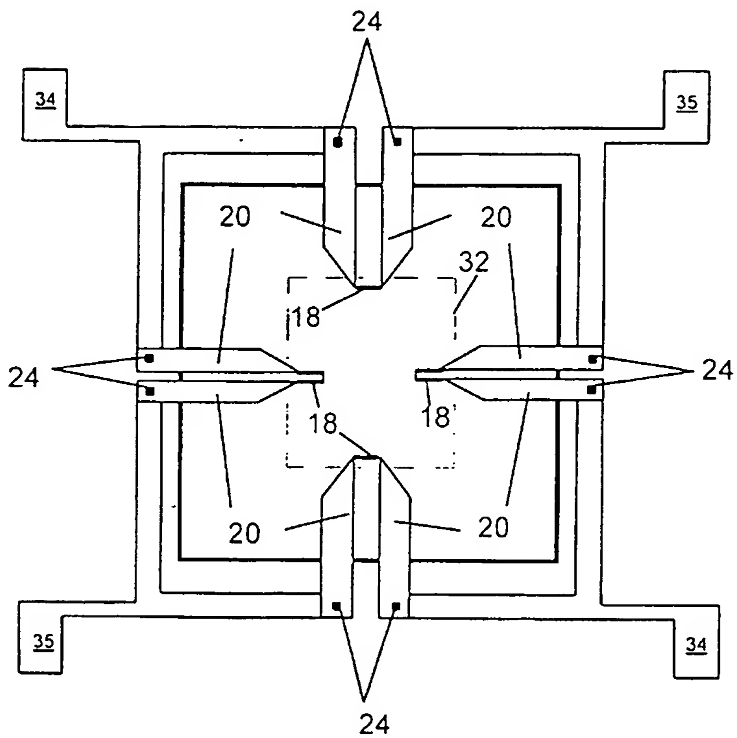


FIGURE 1A



BEST AVAILABLE COPY

FIGURE 2

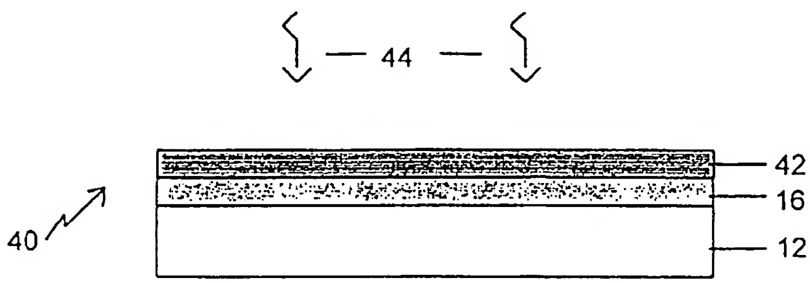


FIGURE 2A

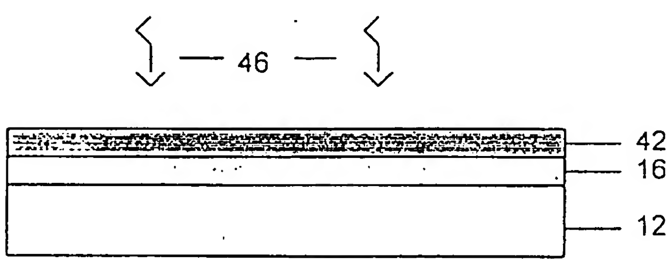


FIGURE 2B

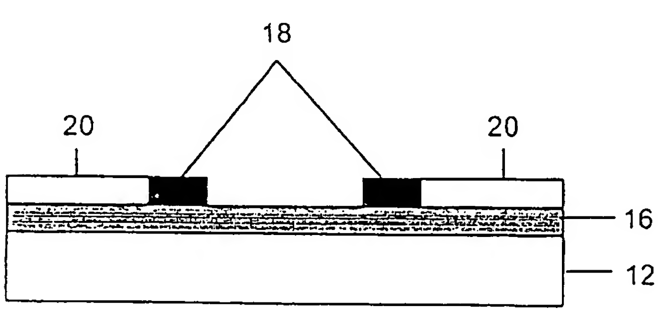


FIGURE 2C

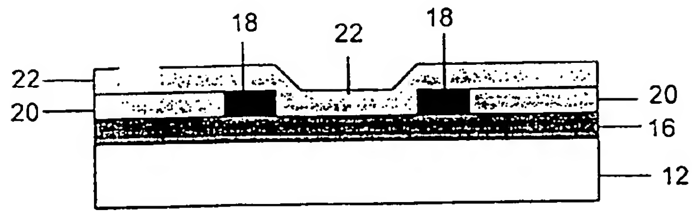


FIGURE 2D

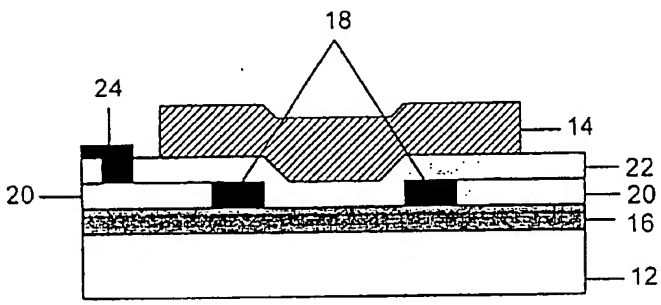


FIGURE 2E